IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A magnetic random access memory (MRAM) cell, comprising:

a first wordline;

a first bitline perpendicular to the wordline; and

a magnetic tunnel junction (MTJ) device disposed at an intersection of the first wordline and the first bitline, the MTJ device having a perpendicular magnetic orientation, the perpendicular magnetic orientation being perpendicular to the wordline and the bitline.

2. (Original) An MRAM cell as recited in claim 1, wherein the MTJ device includes a free layer and a pinned layer, the free layer being closer to the first bitline than the pinned layer.

3. (Original) An MRAM cell as recited in claim 2, further comprising a diode disposed below the MTJ device, the diode being in electrical communication with the first wordline and the pinned layer.

4. (Original) An MRAM cell as recited in claim 1, wherein a second bitline and a third bitline are adjacent to and on either side of the first bitline, and a second wordline and a third wordline are adjacent to and on either side of the first wordline.

5. (Currently amended) An MRAM cell as recited in claim 4, wherein the MRAM cell is ~~programmed~~ programmable by driving current through the second bitline and third bitline, and the second wordline and the third wordline.

6. (Original) An MRAM cell as recited in claim 5, wherein the current driven through the second bitline is in an opposite direction to the current driven through the third bitline.

7. (Original) An MRAM cell as recited in claim 6, wherein the current driven through the second wordline is in an opposite direction to the current driven through the third wordline.

8. (Original) A method for programming a magnetic random access memory (MRAM) cell having a magnetic junction tunnel (MTJ) device with a perpendicular magnetic orientation, comprising the operations of:

driving current in a first direction through a first bitline, the first bitline being adjacent to a second bitline that is in electrical communication with the MRAM cell; and

driving current in a second direction through a third bitline, the third bitline being adjacent to the second bitline and on a side opposite to the first bitline, wherein the second direction is opposite the first direction,

wherein the MRAM cell is programmed to have a first magnetization orientation.

9. (Original) A method as recited in claim 8, wherein driving current in the second direction through the first bitline, and driving current in the first direction through the third bitline programs the MRAM cell to have a second magnetization orientation.

10. (Original) A method as recited in claim 8, further comprising the operations of:

driving current in a third direction through a first wordline, the first wordline being adjacent to a second wordline that is in electrical communication with the MRAM cell; and

driving current in a fourth direction through a third wordline, the third wordline being adjacent to the second wordline and on a side opposite to the first wordline, wherein the fourth direction is opposite the first direction,

wherein the MRAM cell is programmed to have the first magnetization orientation.

11. (Original) A method as recited in claim 10, wherein driving current in the fourth direction through the first wordline, and driving current in the third direction through the third wordline programs the MRAM cell to have the second magnetization orientation.

12 (Original) A method as recited in claim 8, wherein the MRAM cell is read by driving current through the second bitline and driving current through the second wordline.

13. (Original) A method as recited in claim 8, wherein the current flowing in the first direction on the first bitline generates a magnetic field having a first in-plane component, and wherein the current flowing in the second direction on the second bitline generates a magnetic field having a second in-plane component.

14. (Original) A method as recited in claim 13, wherein the first in-plane component cancels out the second in-plane component.

15. (Currently amended) A magnetic random access memory (MRAM) array, comprising:

a plurality of parallel wordlines and parallel bitlines, each ~~bitline~~ of the plurality of bitlines being substantially perpendicular to each of the plurality of wordlines;

a plurality of magnetic tunnel junction (MTJ) devices, each MTJ device disposed at an intersection of one of the plurality of wordlines ~~a wordline~~ and one of the plurality of bitlines ~~a bitline~~, wherein each MTJ device has a perpendicular magnetic orientation, the perpendicular magnetic orientation being perpendicular to each of the plurality of bitlines and each of the plurality of wordlines.

16. (Original) An MRAM array as recited in claim 15, wherein each MTJ device includes a free layer and a pinned layer, the free layer being closer to the bitlines than the pinned layer.

17. (Currently amended) An MRAM cell as recited in claim 16, wherein each MTJ device is in electrical communication with a diode disposed below the MTJ device, each diode being in electrical communication with ~~a wordline~~ one of the plurality of wordlines and the pinned layer of the MTJ device.

18. (Currently amended) An MRAM array as recited in claim 15, wherein each MTJ device is ~~programmed~~ programmable by driving current through two adjacent bitlines and two adjacent wordlines.

19. (Original) An MRAM array as recited in claim 17, wherein current is driven through the adjacent bitlines in opposite directions.

20. (Original) An MRAM array as recited in claim 18, wherein current is driven through the adjacent wordlines in opposite directions.